AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Currently Amended): A method for fabricating trench isolations, comprising:

(a) providing a substrate with a trench therein, the trench comprising an opening;

(b) forming a first dielectric layer on the substrate and filling in the trench by low pressure chemical vapor deposition (LPCVD);

(c) lowering ~~etching~~ the first dielectric layer ~~to lower its surface to~~ below the opening of the trench by performing anisotropic etching and wet etching; and

(d) forming a second dielectric layer on the first dielectric layer and filling the trench to form a trench isolation by high density plasma chemical vapor deposition (HDPCVD) [[;]] .

Claim 2 (Original): The method as claimed in claim 1, wherein step (a) further comprises steps of:

providing the substrate with a pad layer thereon;

defining a pattern on the pad layer;

etching the trench in the substrate using the pattern as a mask;

forming an oxide liner on the bottom and sidewalls of the trench by thermal oxidation; and

forming a nitride liner conformally on the pad layer and the oxide liner.

Claim 3 (Original): The method as claimed in claim 2, wherein the pad layer comprises a pad oxide layer and a pad nitride layer overlying the pad oxide layer.

Claim 4 (Original): The method as claimed in claim 1, wherein the aspect ratio of the trench exceeds 6.

Claim 5 (Original): The method as claimed in claim 1, wherein the first dielectric layer is TEOS.

Claim 6 (Original): The method as claimed in claim 5, wherein the thickness of the first dielectric layer is about 800~3500Å.

Claim 7 (Cancelled).

Claim 8 (Currently Amended): The method as claimed in claim 1, wherein the first dielectric layer is lowered about 100~1000Å~~, by etching, to~~ below the opening of the trench.

Claim 9 (Currently Amended): The method as claimed in claim 1, wherein HDPCVD is successively performed with a relatively low deposition/sputtering ratio and a relatively high deposition/sputtering ratio ~~in order~~.

Claim 10 (Original): The method as claimed in claim 1, wherein the second dielectric layer is a silicon dioxide layer.

Claim 11 (Original): The method as claimed in claim 1, wherein the thickness of the second dielectric layer is about 2500~10000Å.

Claim 12 (Original): The method as claimed in claim 1, further comprising, after HDPCVD, planarizing the dielectric layer and the pad layer.

Claim 13 (Original): The method as claimed in claim 12, wherein the planarizing is performed by CMP.

Claim 14 (Original): The method as claimed in claim 13, wherein the CMP includes slurry-based CMP or fixed abrasive CMP.

Claim 15 (Original): The method as claimed in claim 13, further comprising, after CMP, performing a rapid thermal annealing procedure.

Claim 16 (Currently Amended): A method for fabricating trench isolations, comprising:

(a) providing a substrate with a first trench with a relatively high aspect ratio and a second trench with a relatively low aspect ratio therein, each trench comprising an opening;

(b) forming a first dielectric layer on the substrate and filling the ~~trench~~ trenches by LPCVD;

(c) lowering the surface of the first dielectric layer [[to]] below the openings of the both trenches by etching, wherein the first dielectric layer forms a spacer on the sidewalls of the second trench; and

(d) forming a second dielectric layer on the first dielectric layer and filling both trenches to form trench isolations by HDPCVD [[;]] .

Claim 17 (Original): The method as claimed in claim 16, wherein step (a) further comprises steps of:

providing the substrate with a pad layer thereon;

defining a pattern on the pad layer;

etching a first trench with a relatively high aspect ratio and a second trench with a relatively low aspect ratio in the substrate using the pattern as a mask;

forming an oxide liner on the bottom and sidewalls of both trenches by thermal oxidation; and

forming a nitride liner conformally on the pad layer and the oxide liner.

Claim 18 (Original): The method as claimed in claim 17, wherein the pad layer comprises a pad oxide layer and the pad nitride layer overlying the pad oxide layer.

Claim 19 (Original): The method as claimed in claim 16, wherein the first dielectric layer is TEOS.

Claim 20 (Original): The method as claimed in claim 19, wherein the thickness of the first dielectric layer is about 500~3500Å.

Claim 21 (Currently Amended): The method as claimed in claim 16, wherein the etching is performed by anisotropic etching and wet etching using hydrogen fluoride ~~in order~~.

Claim 22 (Currently Amended). The method as claimed in claim 16, wherein the surface of the first dielectric layer is lowered about 100~1000Å, ~~by etching, to~~ below the opening of the trench.

Claim 23 (Currently Amended): The method as claimed in claim 16, wherein the HDPCVD is successively performed with a relatively low deposition/sputtering ratio and a relatively high deposition/sputtering ratio ~~in order~~.

Claim 24 (Original): The method as claimed in claim 16, wherein the second dielectric layer is a silicon dioxide layer.

Claim 25 (Original): The method as claimed in claim 16, wherein the thickness of the second dielectric layer is about 2500~10000Å.

Claim 26 (Original): The method as claimed in claim 16, further comprising, after HDPCVD, planarizing the dielectric layer and the pad layer.

Claim 27 (Original): The method as claimed in claim 26, wherein the planarizing is performed by CMP.

Claim 28 (Original): The method as claimed in claim 27, wherein the CMP includes slurry-based CMP or fixed abrasive CMP.

Claim 29 (Original): The method as claimed in claim 27, further comprising, after CMP, performing a rapid thermal annealing procedure.